Amendments

1. (Currently Amended) A ferroelectric memory device, comprising:

a main cell array including main bitlines and sub bitlines ~~a bitline structure comprising a main bitline and a sub bitline~~;

a row redundancy cell array configured to share the main bitlines with the main cell array;

a first column redundancy cell array configured to share wordlines and platelines with the main cell array;

a second column redundancy cell array configured to share redundancy wordlines and redundancy platelines with the row redundancy cell array, and to share redundancy main bitlines with the first column redundancy cell array;

~~a main~~ main bitline pull-up ~~controller~~ controllers for pulling up the main bitlines and the redundancy main bitlines in response to first control signals, respectively; and

~~a column~~ column selection ~~controller~~ controllers for connecting data bus lines to the main bitlines and the redundancy main bitlines in response to column selection signals, respectively.

2. (Currently Amended) The device of claim 1, wherein each of the redundancy main ~~bitline~~ bitlines is connected to a redundancy sense amplifier via ~~amplifier viathe redundancy main bitline and~~ a redundancy bus line, and

each of the main ~~bitline~~ bitlines is connected to a main sense amplifier via a main bus line.

3. (Currently Amended) The device of claim 1, wherein the main cell array includes:

~~a main~~ main bitline load ~~controller~~ controllers configured to be connected between a positive power and the main bitlines ~~bitline~~, and to control the flow of current in response to a ~~response toa~~ second control signals, respectively ~~signal~~; and

~~a plurality of~~ main sub cell blocks configured to be serially arranged between the main bitline pull-up ~~controller~~ controllers and the column selection ~~controller, and to have both terminals~~ controllers, and to be connected to the main ~~bitline~~ bitlines at their both end, respectively.

4. (Currently Amended) The device of claim 3, wherein only one of the main bitline load ~~controller~~ controllers is connected ~~one by one~~ to each of the main ~~bitline~~ bitlines.

5. (Currently Amended) The device of claim 3, wherein ~~a plurality of~~ at least two of the main bitline load controllers are connected to ~~one main bitline~~ each of the main bitlines, and evenly placed apart from each other ~~in a predetermined number of sub cell blocks~~.

6. (Currently Amended) The device of claim 1, wherein each of the main bitline pull-up ~~controller~~ controllers is a PMOS transistor having a gate to receive each of the first control signals ~~signal~~, a source connected to a positive power and a drain connected to each of the main ~~bitline~~ bitlines.

7. (Currently Amended) The device of claim 1, wherein each of the column selection ~~controller~~ controllers is a transmission gate having a gate to receive each of the column selection signals ~~address signal~~, and both terminals connected to each of the data bus ~~line~~ lines and each of the main bitlines ~~bitline~~, respectively.

8. (Currently Amended) The device of claim 3, wherein each of the main bitline load ~~controller~~ controllers is a PMOS transistor having a gate to receive each of the second control signals ~~signal~~, a source connected to a positive power, and a drain connected to each of the main ~~bitline~~ bitlines.

9. (Currently Amended) The device of claim 3, wherein each of the main sub cell blocks ~~block~~ includes:

a sub bitline configured to be connected in common to a plurality of unit memory cells~~,~~ ~~each unit memory cell~~ each of which is connected to each of the wordlines and each of the platelines, respectively ~~a wordline and a plateline~~;

a first NMOS transistor having a gate connected to a first terminal of the sub bitline, and a drain connected to each of the main ~~bitline~~ bitlines;

a second NMOS transistor having a gate connected to a third control signal, a drain connected to a source of the first NMOS transistor, and a source connected to ground;

a third NMOS transistor having a gate connected to a fourth control signal, a drain connected to a second terminal of the sub bitline, and a source connected to ground;

a fourth NMOS transistor having a gate connected to a fifth control signal, a source connected to the second terminal of the sub bitline, and a drain connected to a sixth control signal; and

a fifth NMOS transistor having a gate connected to a seventh control signal, a drain connected to each of the main bitlines ~~bitline~~, and a source connected to the second terminal of the sub bitline.

10. (Currently Amended) The device of claim 9, wherein the row redundancy cell array ~~includesa plurality of~~ includes sub row redundancy cell blocks, wherein each of the sub row redundancy cell ~~block~~ blocks has both terminals connected to each of the main ~~bitline~~ bitlines, respectively.

11. (Currently Amended) The device of claim 10, wherein each of the sub row redundancy cell ~~block~~ blocks having the same structure as that of each of the main sub cell ~~block~~ blocks includes the same number of unit memory cells as that of each of the main sub cell blocks ~~block~~, and

wherein ~~a redundancy wordline and a redundancy plateline~~ redundancy wordlines and redundancy platelines connected to a predetermined number of the unit memory cells are grounded.

12. (Currently Amended) The device of claim 10, wherein each of the row redundancy sub cell ~~block~~ blocks having the same structure as that of each of the main sub cell ~~block~~ blocks includes a smaller number of unit memory cells than that of ~~corresponding unit memory cells in~~ each of the main sub cell blocks ~~block~~, and

wherein each of the row redundancy sub cell ~~block~~ blocks further includes a capacitor connected between ground and a sub bitline in the row redundancy sub cell block.

13. (Original) The device of claim 12, wherein the capacitor is a NMOS transistor having a gate connected to the sub bitline, a drain and a source connected to ground.

14. (Original) The device of claim 12, wherein the capacitor is a NMOS transistor having a gate connected to ground, a drain and a source connected to the sub bitline.

15. (Original) The device of claim 12, wherein the capacitor is a diode having an anode connected to ground, and a cathode connected to the sub bitline.

16. (Original) The device of claim 12, wherein the capacitor is a ferroelectric memory device.

17. (Currently Amended) The device ~~ofone~~ of claim ~~10, wherein~~ 9, wherein the first column redundancy cell array includes ~~a plurality of~~ first unit cell blocks, each of the first unit cell blocks ~~arrays including redundancy main bitlines, respectively, each first unit cell array~~ having the same structure as each of the main sub cell blocks ~~that of the corresponding main cell array~~.

18. (Currently Amended) The device of claim 10, wherein the second column redundancy cell array ~~includesa plurality of~~ includes second unit cell ~~arrays, each second unit cell array configured to share the redundancy main bitline with the first unit cell array and to have~~ blocks, each of the second unit cell blocks having the same structure as ~~that~~ each of ~~the row~~ the sub row redundancy cell blocks ~~array~~.

19. (Cancelled)

20. (Original) A ferroelectric memory device, comprising:

(1) a main cell array, including:

(A) a main bitline load controller configured to be connected between a main bitline and a positive power, and to control the flow of current in response to a second control signal, and

(B) a plurality of main sub cell blocks, each main sub block having both terminals connected to the main bitline, including:

(a) a sub bitline connected in common to a plurality of unit memory cells connected to a wordline and a plateline,

(b) a first NMOS transistor having a gate connected to a first terminal of the sub bitline and a drain connected to the main bitline,

(c) a second NMOS transistor having a gate connected to a third control signal, a drain connected to a source of the first NMOS transistor, and a source connected to ground,

(d) a third NMOS transistor having a gate connected to a fourth control signal, a drain connected to a second terminal of the sub bitline, and a source connected to ground,

(e) a fourth NMOS transistor having a gate connected to a fifth control signal, a source connected to the second terminal of the sub bitline, and a drain connected to a sixth control signal, and

(f) a fifth NMOS transistor having a gate connected to a seventh control signal, a drain connected to the main bitline, and a source connected to the second terminal of the sub bitline;

(2) a row redundancy cell array configured to share main bitlines with the main cell array;

(3) a first column redundancy cell array configured to share wordlines and platelines with the main cell array and to include redundancy main bitlines;

(4) a second column redundancy cell array configured to share redundancy wordlines and redundancy platelines with the row redundancy cell array, and to share redundancy main bitlines with the column redundancy cell array;

(5) a main bitline pull-up controller for pulling up main bitlines and redundancy main bitlines in response to first control signals, respectively;

(6) a column selection controller for connecting the main bitlines to redundancy columns and the redundancy main bitlines to main columns in response to column selection signals, respectively;

(7) a data bus unit shared by the redundancy column and the main column;

(8) a redundancy bus connected to the data bus unit shared by the redundancy column;

(9) a main bus connected to the data bus unit shared by the main column;

(10) a redundancy sense amplifier array connected to the redundancy bus; and

(11) a main sense amplifier array connected to the main bus.